JSST
Journal of Space Science and Technology

P-ISSN: 2008-4560
E-ISSN: 2423-4516

Journal of Space Science and Technology

Vol. ??, No. ??, pp.1-8, ????
https://doi.org/ 10.22034/jsst.2025.1567
Journal Homepage: https://jsstpub.com

Original Research Paper

Design and Performance Analysis of a 1.8 GHz Low-Noise Amplifier for GSM Receivers

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ARTICLE INFO

Article History:

Receive 10 August 2025
Revise 24 October 2025
Accept 25 October 2025
Available Online 03 November 2025

Keywords:

LNA
Frequency
Noise figure
inductive
cascoded

ABSTRACT

Low Noise Amplifiers (LNAs) play a vital role in communication systems, especially in the receiver section, as they amplify weak received signals with minimal noise. These amplifiers come in various types, but the common-source structure with inductive degeneration is considered one of the most widely used topologies in this field due to its optimal balance between noise figure, gain, and input impedance matching. In this article, the design and simulation of an LNA for the 1.8 GHz GSM band with the aim of achieving high gain, a noise figure of less than 2 dB, and low power consumption are presented. The designed structure utilizes inductive peaking techniques, cascoded configuration to improve stability and isolation, and impedance matching networks. The simulations were conducted using the Cadence Virtuoso tool with the SpectreRF simulator, based on TSMC 0.18 µm RF CMOS technology, with S-parameter and linear and nonlinear analyses. The results show that the designed amplifier has a gain of 17.88 dB, a noise figure of 1.87 dB, and a power consumption of 4.3 mW, making it suitable for sensitive RF applications, especially in mobile devices and base stations.

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How to Cite this Article:
A. Panahgholi, A. Eteghad, and E. Najafiaghdam, "Design and performance analysis of a 1.8 GHz low-noise amplifier for GSM receivers," *Journal of Space Science and Technology*, Vol. ??, NO. ??, pp. 1-8, ????, https://doi.org/ 10.22034/jsst.2025.1567.

NOMENCLATURE

Abbreviation	Full Form
μf	Stability Factor (μ-factor)
Kf	Rollett Stability Factor
RF	Radio Frequency
TT	Typical–Typical (Process Corner)
FF	Fast–Fast (Process Corner)
SS	Slow–Slow (Process Corner)
IIP3	Input Third-Order Intercept Point
LNA	Low Noise Amplifier
P1dB	1 dB Compression Point
VCCS	Voltage-Controlled Current Source
S-parameter	Scattering Parameter

Symbol	Description	Unit
R_s	Source Resistance	Ω
R_g	Gate Resistance	Ω
R_{Lg}	Inductor Loss Resistance	Ω
R_p	Parallel Load Resistance	Ω
R_o	Output Resistance	Ω
Z_{in}	Input Impedance	Ω
$\overline{i_{n,total}^2}$	Total Input Noise Current	A²/Hz
g_m	Transconductance	S
ω_T	Transition Angular Frequency	rad/s
ω	Angular Frequency	rad/s
L_g	Gate Inductor	nH
L_s	Source (Degeneration) Inductor	nH
k	Boltzmann's Constant	J/K
T	Temperature	K
Δf	Bandwidth	Hz
C_{gs}	Gate–Source Capacitance	F
NF	Noise Figure	dB
A_v	Voltage Gain	—
F	Noise Factor	—
$F_{cascode}$	Cascode Noise Contribution	—
γ	Excess Noise Factor	—
γ_{gd}	Drain–Gate Noise Coefficient	—
Δ	Determinant of S-parameters	—

1. INTRODUCTION

Low noise amplifiers (LNAs) are an important part of communication systems, especially in the front-end of the receiver. At the receiver, they amplify weak signals while providing minimal noise [1]. This article presents the design and simulation of an LNA operating at a frequency of 1.8 GHz, focusing on achieving a noise figure (NF) of less than 2 dB and high gain [2], [3]. The application for this LNA is in wireless communication systems, particularly in mobile devices and base stations that operate within the GSM frequency band (1.8 GHz) [4].

LNAs are the first important component at the receiver side that determines the overall performance of the system [5]. In LNA design, several important characteristics, such as achieving low noise figure, high gain, and proper impedance matching at the input/output, must be considered [6]. Noise figure is one of the most important parameters in LNAs because it directly affects the receiver sensitivity, while the gain value determines the overall dynamic range of the system [2].

One of the common LNA structures used in wireless communication systems is the degenerate inductive common source amplifier [7]. An interesting feature of this type of structure is that it provides a good balance between noise figure, gain, and input impedance matching [8]. The inductive degeneration used in this type of structure improves the input impedance matching and reduces the noise figure [9]. Cascoded structures can also be used to increase reverse isolation and improve the stability of the LNA [7].

Various techniques have been selected in the design of LNA for proper performance, including the use of inductive decay, cascade configuration, and noise cancellation techniques [10]. Input and output impedance matching networks will be used to ensure the matching rate, which will increase the power transfer in the design [4]. The design of the bias circuit is also an important part to operate at the appropriate DC operating point and thus the stability of the LNA [11].

After designing the LNA for the desired values, the circuit is simulated using the advanced circuit simulation tool Cadence Virtuoso. After designing the LNA for the desired values, the circuit is simulated using the advanced circuit simulation tool Cadence Virtuoso. The simulation results will help evaluate the performance of the LNA in terms of noise figure, gain, input/output matching, and stability.

2. DESIGN METHODOLOGY

Designing an LNA with low noise figure and high gain requires a thorough analysis of noise figure parameters, impedance matching, and the

selection of an appropriate topology. In this design, a common-source structure with inductive degeneration and cascoded configuration has been used, which is widely applied in RF amplifiers due to advantages such as proper input matching, low noise, and high isolation.

The noise figure of the proposed LNA can be derived from the Friis formula [12], considering the contributions from the channel noise of M1 ($i_{n,M1}^2 = 4kT\gamma g_m \Delta f$), induced gate noise, and losses from the inductors and cascode stage [13], [14]. The total noise factor F (with $NF = 10\,log_{10}\,F$) can be expressed using Eq. (1):

$$F = 1 + \frac{\overline{i_{n,total}^2}}{4kTR_s g_m^2 \Delta f} = 1 + \frac{\gamma}{g_m R_s} + \frac{R_g + R_{Lg}}{R_s} + \gamma_{gd}(\frac{\omega}{\omega_T})^2 + F_{cascode} \quad (1)$$

where $k = 1.38 \times 10^{-23} J/K$ is Boltzmann's constant, $T = 300\,K, R_g = 1/5g_m$ is the gate resistance, $R_{Lg} = \omega L_g/Q$ is the inductor loss, γ_{gd} is the drain-gate noise coefficient, and $\omega_T = g_m/C_{gs}$ is the transition frequency. The term $F_{cascode} \approx 1 + (g_{m2}R_s/5)$ accounts for the cascode noise contribution.

For the operating frequency of 1.8 GHz, where $R_g \ll R_s$ and $\omega/\omega_T \ll 1$, the above expression simplifies to the commonly used approximate form [14], as shown in Eq. (2):

$$NF \approx \frac{\gamma}{g_m R_s} + 1 \quad (2)$$

where γ is the excess noise factor of the transistor (typically 2/3–2.5 for CMOS, unitless), g_m is the transconductance of the input transistor, and R_s is the source resistance (usually 50 Ω).

To reduce the noise figure, g_m must be increased, which can be achieved by increasing the transistor width or bias current, but this increase can lead to higher power consumption. Therefore, a design balance has been considered between the noise figure and power consumption.

To match the input impedance with a 50 Ω source, the discharge inductor L_s and gate inductor L_g have been used. The input impedance of the structure can be derived from the small-signal model of M1 (as a VCCS with C_{gs}, $g_m V_s$, neglecting C_{gd} initially) [14], given by full the expression Eq. (3):

$$Z_{in} = j\omega L_g + \frac{1}{j\omega C_{gs}} + \frac{j\omega L_s + \frac{1}{g_m}}{1 + j\omega\frac{C_{gs}}{g_m} + (j\omega)^2 L_s C_{gs}} \quad (3)$$

Where the real part includes loop effects and C_{gs}(gate-source capacitance, F). This full expression simplifies to the approximate because $1/g_m \ll \omega L_s$ (large g_m, strong Degeneration), and C_{gd} is negligible, yielding Eq. (4) [14]:

$$Z_{in} \approx j\omega L_g + \frac{1}{g_m + j\omega L_s} \quad (4)$$

To achieve precise impedance matching, the imaginary part of this impedance must be matched to 50 Ω. In this design, the values of L_s and L_g are considered to be 5 nH and 90 nH, respectively, which result in proper input matching at the center frequency of 1.8 GHz.

The circuit gain can be calculated based on the small-signal model and the overall gain of the cascoded structure, derived from the voltage gain $A_v = V_{out}/V_{in}$ where current $g_m V_s$ flows into the load ($R_d \parallel r_{o2} \parallel r_{o4}$, tuned by L_d) [14], given by the full expression in Eq. (5):

$$A_v = -g_m(R_d \parallel r_{o2} \parallel r_{o4}) \cdot \frac{Z_{load}}{Z_{source}} \approx -g_m R_p \quad (5)$$

(dimensionless, converted to dB). This full expression simplifies to the approximate, assuming high output resistance ($r_{o2}, r_{o4} \gg R_d$) and tuned load(cascode reduces Miller effect), leading to Eq. (6)[14]:

$$Gain \approx g_m \cdot R_o \quad (6)$$

where R_o includes the load resistance R_L and the equivalent output impedance of the upper transistor in the cascaded (Ω). In this design, the calculated gain value is approximately 18.2 dB.

The circuit is designed and simulated using TSMC 0.18 µm RF CMOS technology. The transistor models are rfnmos2v and rfpmos2v, based on the official factory models.

2.1 Design specifications

The transistors designed for this circuit have been selected to provide optimal performance at high frequencies. The design parameters of each transistor are presented in Table 1:

Table 1. w/l size of designed transistors.

	W/L (μm/μm)
M_1	56.25/0.18
M_2	62.5/0.18
M_3	152.5/0.18
M_4	134.2/0.18
M_5	31.25/0.18
M_6	93.75/0.18

The parameters related to inductors, resistors, with a 1.8V power supply are also presented in Tab. 2 & Tab. 3. Because the input inductors (L_{g1} and L_{g4}) have a high value, they are implemented off-chip to achieve the desired impedance matching at the specified frequency, while the other inductors are of the on-chip spiral type.

Table 2. Designed inductor values.

	(nH)
L_1	0.68
L_4	1.78
L_{g1}	90
L_{g4}	30
L_L	5

Table 3. Designed resistor values.

	(Ω)
R_L	500
R_b	430
R_x	10 k

3. SIMULATION

To evaluate the performance of the designed low-noise amplifier, the circuit simulation in Fig. 1 was conducted to examine the values of S-parameters, noise figure, and nonlinear analyses. All simulations were performed in the Cadence Virtuoso software environment using the SpectreRF simulator.

Figure 2 shows the input matching of the circuit with a 50 Ω source. The simulated value for S_{11} at a frequency of 1.8 GHz is approximately -16.24 dB, indicating a very good match. This result also aligns with the theoretical analysis, as the input impedance matching conditions have been met using the gate inductor ($L_g = 90\,nH$) and the discharge inductor ($L_s = 5\,nH$).Minor differences from the ideal value are due to the presence of modeled interference in the simulation environment. In the frequency range of 1 to 4 GHz, the behavior of the circuit dispersion parameters (S-parameters) is quite stable. The forward gain (S_{21}) reaches a maximum value of about 9 dB at the center frequency of 1.8 GHz and remains above −2 dB up to about 2.8 GHz, indicating a wideband response and a satisfactory gradual roll-off after the center frequency.

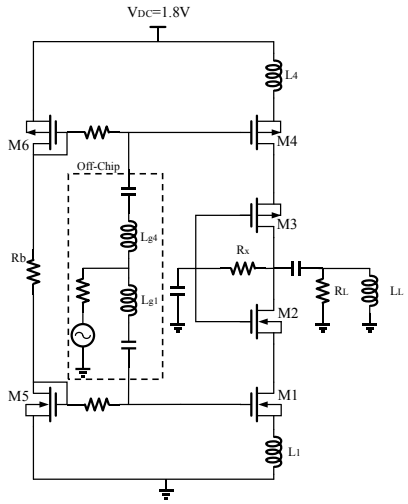

Fig. 1. Proposed LNA schematic including off-chip input inductors.

The reverse isolation (S_{12}) is lower than −40 dB throughout the band, indicating the favorable performance of the cascode structure in preventing reverse feedback. The output reflection coefficient (S_{22}) also remains better than −6 dB up to 4 GHz, indicating an acceptable output matching of the circuit.

All simulations of circuit parameters, including dissipation parameters (S_{11}, S_{12}, S_{22}, S_{21}), input impedance (Z_{11}), noise figure, and available gain, have been performed in the frequency range of 1 to 4 GHz to investigate the circuit performance over the full frequency range. All simulations were initially performed under typical process conditions (TT). To assess the stability of the circuit against process variations, simulations were also performed at FF and SS corners. The difference between the noise figure and the available gain obtained was less than 2 dB, indicating the stability of the circuit performance. The values reported at 1.8 GHz are for the center point of the circuit performance.

Figure 3 shows that the real part of the input impedance curve is around 50 Ω and the imaginary part is close to zero, indicating the achievement of impedance matching conditions at the design center

frequency (1.8 GHz).This result confirms that the values of the reactive elements are well-tuned and the common-source structure with inductive discharge has provided the desired performance.

The noise figure at the central frequency was measured to be approximately 1.87 dB, which aligns with the expected value based on theoretical relations. According to Eq. (2), it was expected that the noise figure would be less than 2 dB, which has also been confirmed in the simulation. In Fig. 4, the noise figure of 1.877dB indicates the optimal design of the input section and the correct selection of transistor parameters.

The circuit's available gain According to Fig. 5, a value of approximately 17.88 dB was obtained in the simulation, which only slightly differs from the theoretically calculated value (approximately 18.2 dB).This slight difference is due to the more accurate modeling of passive elements and parasitic effects, and it falls within an acceptable range. This level of gain well demonstrates the proposed LNA's ability to amplify weak signals.

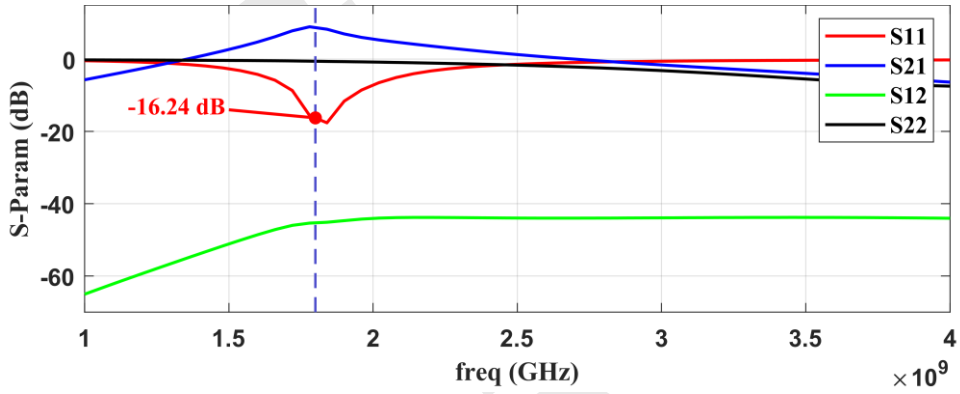

Fig. 2. Simulated S-parameters of the proposed LNA, with S_{11} highlighted at 1.8 GHz (−16.24 dB).

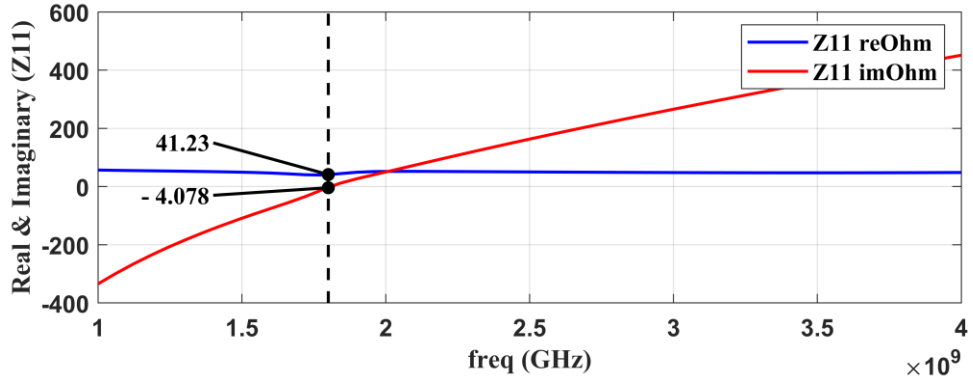

Fig. 3. Input impedance matching at 1.8 GHz: real ~50 Ω and imaginary ≈ 0..

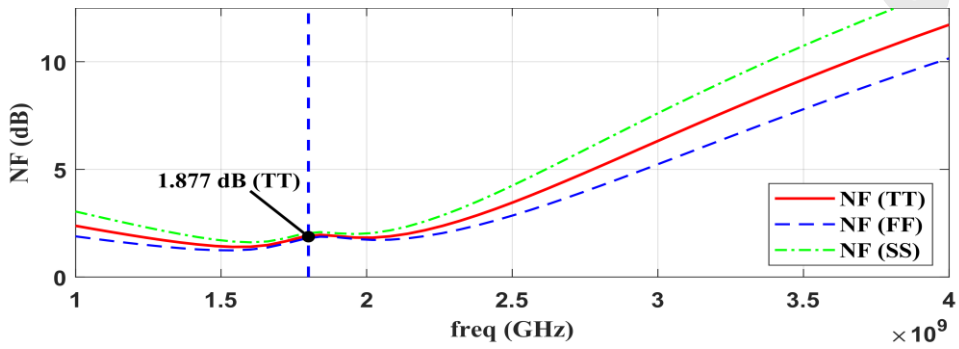

Fig. 4. Simulated noise figure (NF) for TT, FF, and SS corners. The TT value of 1.87 dB at 1.8 GHz is highlighted as the reference point.

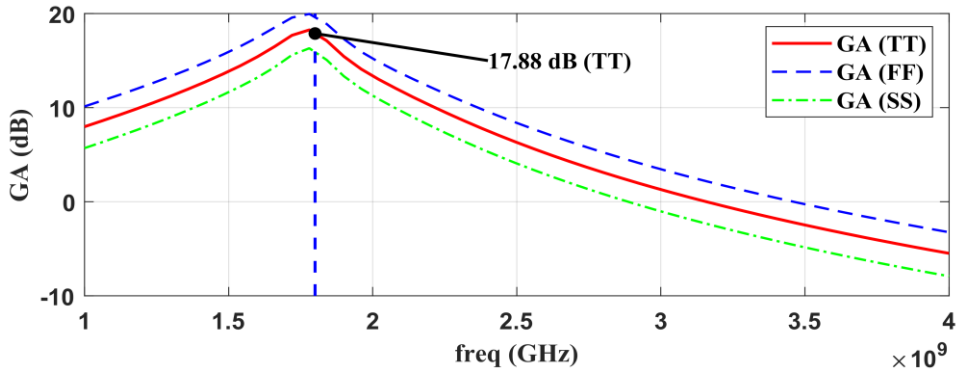

Fig. 5. Simulated available gain (GA) for TT, FF, and SS corners. The TT value of 17.88 dB at 1.8 GHz is highlighted as the reference point.

The third-order intersection point (IIP3) is obtained as shown in Fig. 6. To perform the two-tone test, two signals with frequencies of 1.8 GHz and 1.9 GHz (with a difference of $\Delta f = 100$ MHz) were applied to the circuit input. The input power was varied from −30 dBm to determine the linear and nonlinear regions of the circuit performance. As a result, we plotted the principal component (first-order) with a slope of 1 dB/dB and the third-order component (IM3) with a slope of 3 dB/dB against the input power. The intersection point of these two curves shows the value of IIP3 = −15.9 dBm, which indicates the optimal performance of the circuit in terms of maintaining linearity and resistance to strong signals in high-frequency applications.

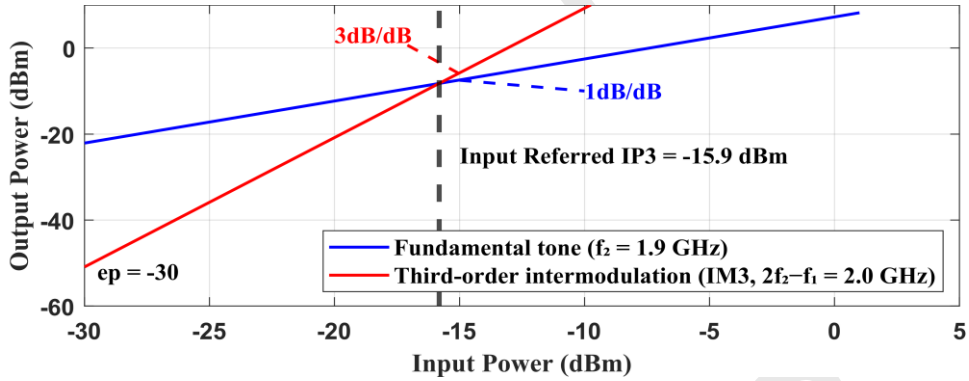

Fig. 6. Simulated two-tone test for third-order intercept point (IIP3). The intersection of the fundamental and third-order components yields an IIP3 of −15.9 dBm.

Figure 7 shows the 1 dB compression point (P1dB). This point indicates how much the circuit can amplify the signal without entering the nonlinear region. The obtained P1dB value is −25.83 dBm for the input referred to at 1.8 GHz, which is considered acceptable given the low-power structure of the circuit.

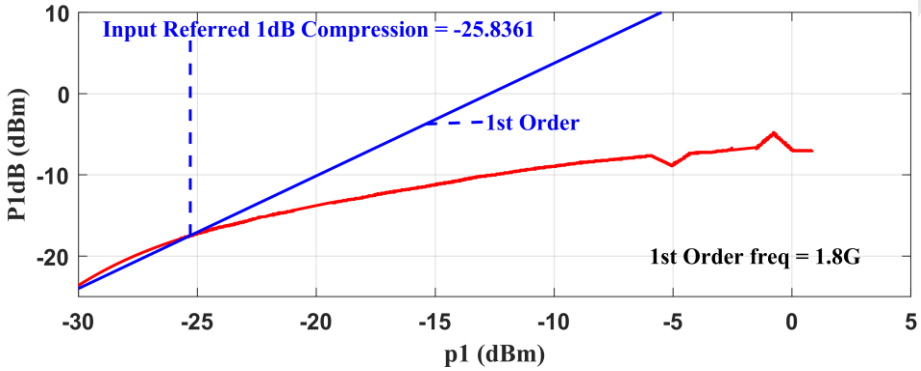

Fig. 7. Simulated 1 dB compression point (P1dB) at 1.8 GHz, showing an input-referred P1dB of −25.83 dBm.

To ensure the stability of the circuit across the entire operating frequency range, the roulette stability factors (K) and μ were extracted based on the dispersion parameters (S-parameter). The μ factor was calculated and plotted according to Eq. (7)[15].

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta^* S_{11}^*|^2 - |S_{12}S_{21}|^2}, \quad \Delta = S_{11}S_{22} - S_{12}S_{21} \tag{7}$$

As illustrated in Fig. 8, simulations conducted from 1 to 4 GHz demonstrate that the K factor remains above 1 throughout this frequency range, varying between approximately 3.8 at 1.72 GHz and 6.6 at 4 GHz. This indicates the overall stability of the circuit at all frequencies. On the other hand, the μ factor is less than 1 (between 0.166 and 0.748) at lower frequencies (from 1 to about 1.78 GHz). This means that the circuit input is conditionally stable and may be sensitive to changes in source impedance within this range. But μ is always greater than 1 after the circuit's center frequency (about 1.8 GHz), going from about 1.1 at 1.78 GHz to about 10.35 at 4 GHz. This reflects an improvement in the stability margin and indicates unconditional stability at higher frequencies. Although there are slight fluctuations in μ in the intermediate region (notably values below 1 at around 1.96 and 2.02 GHz), these do not affirm absolute stability across the entire band but rather ensure optimal performance in the primary operating band (from the center frequency onward).

Considering these results and adhering to standard stability criteria (which necessitate K > 1 and μ > 1 throughout the entire band for unconditional stability)[15], the designed circuit is assessed as absolutely stable at frequencies above the center frequency, with no unstable regions present. In contrast, at lower frequencies, conditional stability is observed, necessitating careful impedance matching to avoid potential oscillations.

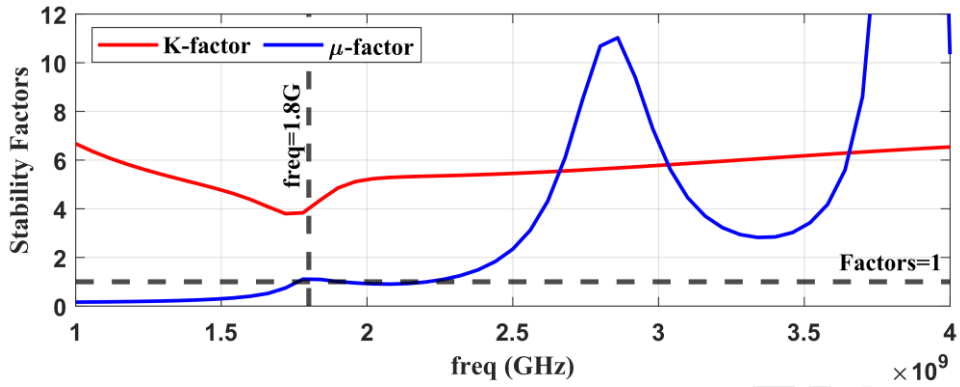

Fig. 8. Simulated K and μ factors confirming stability across the band.

4. CONCLUDING REMARKS

The results obtained from the simulations indicate that the proposed design has achieved a suitable noise figure and gain alongside very low power consumption. The improvement in the linearity of the amplifier, considering the IIP3 value, is also noteworthy. This ensures that the circuit maintains operational stability in the presence of high-power signals and prevents nonlinear distortion.

Furthermore, the extracted stability factors (K and μ) confirm that the amplifier remains unconditionally stable above the center frequency, ensuring reliable operation across the intended frequency band.

Comparison with similar designs available in the literature shows the relative superiority of this structure, particularly in terms of gain, NF, and power consumption. Additionally, the agreement of the simulation results with theoretical values confirms the accuracy of the design and simulation.

CONFLICTS OF INTEREST

The authors declare that they have no conflict of interest.

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